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Comparison among different CMOS inverter for Low leakage at different Technologies

Vijay Kumar Sharma[1], Surender Soni[2]
1- Department of Electronics & Communication, College of Engineering, Teerthanker Mahaveer University, Moradabad
2- Department of Electronics & Communication, National Institute of Technology, Hamirpur
vijay.buland@gmail.com

ABSTRACT

In CMOS circuits, the reduction of the threshold voltage due to voltage scaling leads to increase in sub threshold leakage current and hence, static power dissipation. In the nanometer technology regime, power dissipation and Process parameter variations have emerged as major design considerations. These problems continue to grow with leakage power becoming a dominant form of power consumption. On the other hand, variations in the device parameters, both systematic and random, translate into variations in circuit parameters like delay and leakage. Leakage power dissipation is projected to grow exponentially in the next decade according to the International Technology Roadmap for Semiconductors (ITRS). This directly affects portable battery operated devices such as cellular phones and PDAs since they have long idle times. Several techniques used that efficiently minimize this leakage power loss. Stacking is a leakage reduction technique.

Key words: Low Power, Leakage, CMOS inverter

1. Introduction

As technology scales down, the size of transistors has been shrinking. The number of transistors on chip has thus increased to improve the performance of circuits. The supply voltage, being one of the critical parameters, has also been reduced accordingly in order to maintain the characteristics of an MOS device. Therefore in order to maintain the transistor switching speed, the threshold voltage is also scaled down at the same rate as the supply voltage. As a result, leakage currents increase dramatically with each technology generation [2,6]. As the leakage current increases faster, it will become more and more proportional to the total power dissipation.

$$P_{LEAK} = I_{LEAK} * V_{dd} \quad \ldots\ldots\ldots\ldots\ldots (1)$$

Designers need to develop new low power techniques to reduce total leakage in nano-scale circuits, especially for chips that are used in power-constrained portable systems. The leakage current consists of reverse-bias diode currents and sub-threshold current. The former is due to the stored charge between the drain and bulk of active transistors while the later is due to the carrier diffusion between the source and drain of the off transistors. The sub threshold current is given as:

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$$Ids = \mu_{oCox} \frac{W}{1}(m-1)\ (Vt)^2\ e(Vgs-Vth)/mVt_*\ (1\text{-}e\text{-}Vds/Vt) \quad \ldots (2)$$

Where:

$$m = 1 + \frac{Cdm}{Cox} = 1 + \frac{3tox}{Wdm} \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Where:

Vth = The threshold voltage
Vt = The thermal voltage
Cox = Gate oxide capacitance
μ_0 = Zero bias mobility
m = The sub threshold swing coefficient (also called body effect coefficient)
Wdm= The maximum depletion layer width
tox = The gate oxide thickness
Cdm = The capacitance of the depletion layer

In order to facilitate voltage scaling without affecting the performance, threshold voltage has to be reduced. This also leads to better noise margins and helps to avoid the hot-carrier effects in short channel devices. Scaling down of threshold voltage results in exponential increase of the sub-threshold leakage current. So, before going to in nanometer regime we need some techniques applied for CMOS logic to minimize the leakage power. Stacking is such technique used for minimize the leakage power [1].

2. Leakage reduction by stacking of transistors

Sub threshold leakage is exponentially related to the threshold voltage of the device and the threshold voltage changes due to body effect. From these two facts, one can reduce

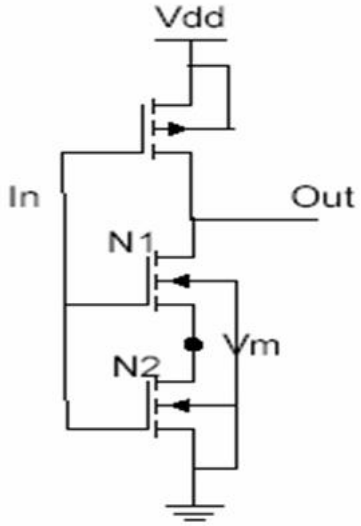

Figure 1: Block diagram

the sub-threshold leakage in the device by stacking two or more transistors serially. The transistors above the lowest transistor will experience a higher threshold voltage due to the difference in the

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voltage between the source and body. Also, the Vds of the higher transistor is decreased, since the intermediate node has a voltage above the ground. These results in reduction of DIBL affect hence better leakage savings. However, forced stack devices have strong performance degradation that be taken into account when applying the techniq ue. Figure (1) shows an inverter with a forced NMOS stack. It is evident that the aforementioned ef fects are explained by looking at the threshold voltage and leakage values of this inverter. The leakage savings is large when the conventional inverter and the forced NMOS, fo rced PMOS case are compared. The new threshold voltage of the device varies this fact. The node voltage at Vm does the following:

1. Increases N1's threshold voltage due to body effect,
2. Increases N1 and N2's threshold voltage due to lower Vds (lower DIBL), Puts N1 into strong off state since Vgs is negative

From above, it was seen that the sub-threshold leakage also strongly depends on the input applied to the circuit. This creates another method for reducing sub-threshold leakage.

3. Result and Discussion

The implemented circuits are simulated to measure total leakage Power. Technique using 70 nm, 100 nm, 130, 180 nm technology has been simulated on TSPICE tool. Tables show the simulation results of each circuit at room temperature. Using leakage monitoring and the balance between sub-threshold leakage and BTBT (band to band tunneling) leakage, the new optimal body bias technique gives reduction in total leakage power. Since the optimal bias results in the minimum leakage current for nano-scale device in standby mode, the power in active mode is also improved by applying the optimal body bias. The circuits for CMOS inverter are shown below and their corresponding total leakage power vs. technology is listed in the tables.

In stacking of transistors we vary the threshold voltage of the transistors by providing bulk to source biasing negative [3]. This increase the threshold voltage of the device, more threshold voltage means less sub threshold current, this cause less total leakage power. The threshold voltage of a device is given as:

$$V_{th} = V_{fb} + 2\psi B + \frac{\sqrt{2\varepsilon siqN_a(2\psi B + V_{bs})}}{C_{ox}} \quad \ldots\ldots\ldots\ldots\ldots\ldots(4)$$

Where:

Vfb = The flat-band voltage
Na = The doping density in the substrate
ψB = The difference between the Fermi potential and the intrinsic potential in the substrate

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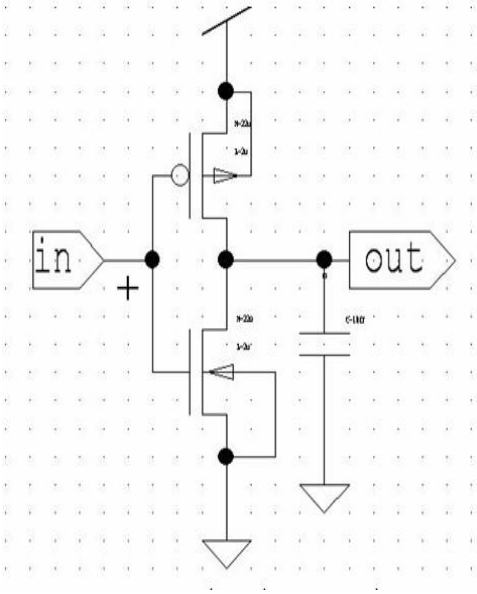


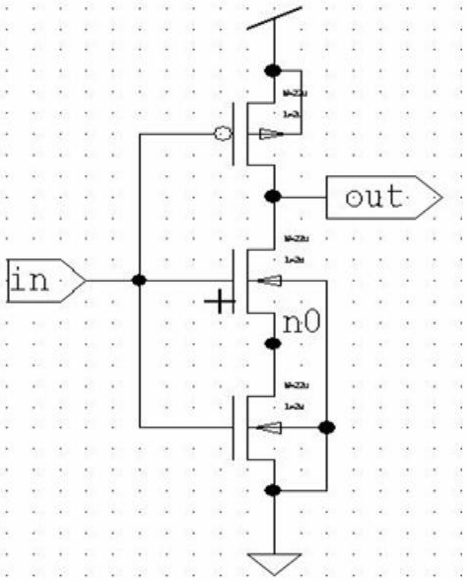
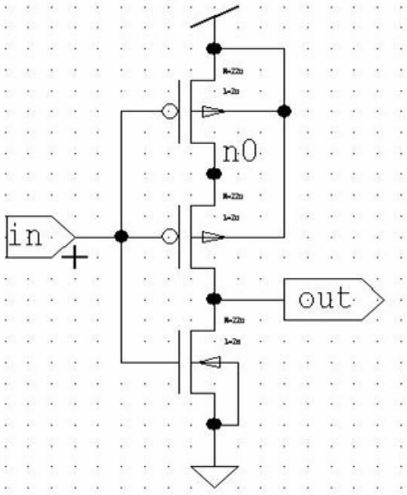


Figure 2: Conventional CMOS inverter **Figure 3:** Forced NMOS transistor CMOS inverter



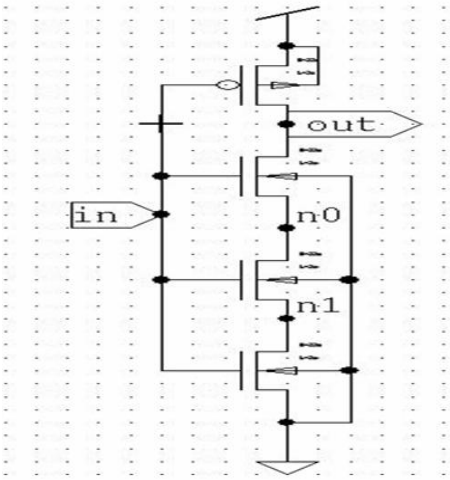


Figure 4: Forced PMOS transistor CMOS transistors Figure (5) Forced 2-NMOS CMOS inverter

Table 1: For conventional CMOS inverter

Technology (nm)	Total leakage power (nW)
70	8.1478
100	1.8172
130	0.3635
180	0.2873

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Table 2: For forced NMOS transistor CMOS inverter

Technology (nm)	Total leakage power (nW)
70	1.2271
100	0.1495
130	0.0897
180	0.0371

Table 3: for forced PMOS transistor CMOS inverter

Technology (nm)	Total leakage power (nW)
70	2.8180
100	1.0102
130	0.2364
180	0.1278

Table 4: for forced 2-NMOS transistors CMOS inverter

Technology (nm)	Total leakage power (nW)
70	0.5798
100	0.0761
130	0.0525
180	0.0112

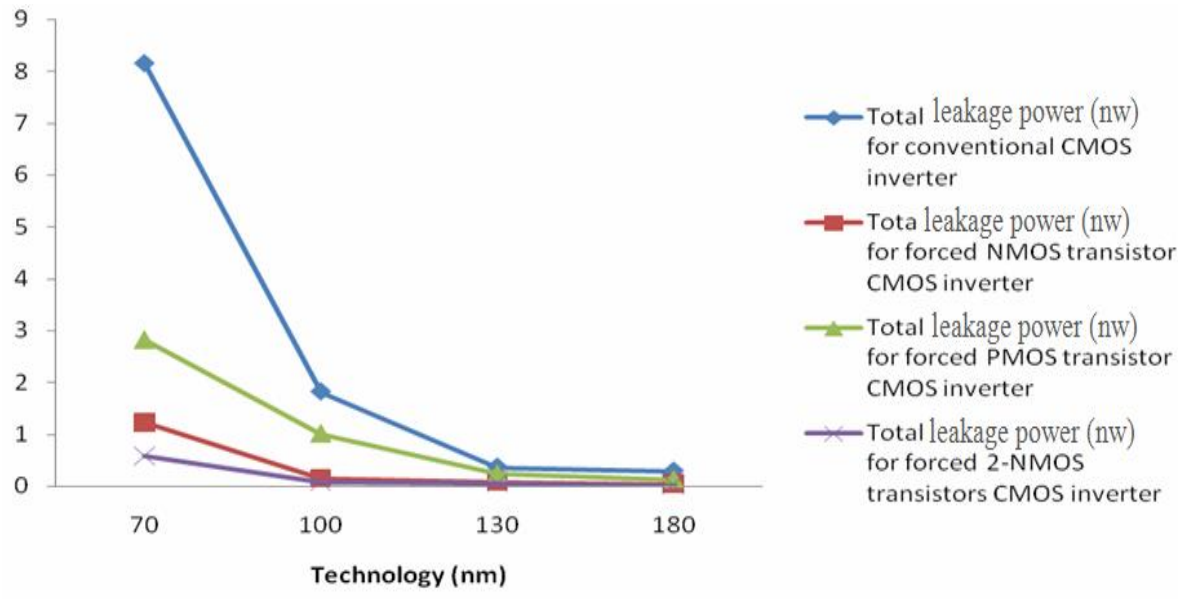

Figure 6: Total leakage power (nW) Vs Technology (nm)

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4. Conclusion

Scaling down of device dimensions, supply voltage and threshold voltage for achieving high-performance and low dynamic power dissipation has largely contributed to the increase in leakage power dissipation. We have presented an efficient design methodology for reducing the leakage power in CMOS inverter circuit. Implications of technology scaling on the choice of techniques to mitigate total leakage are examined. The results are guidelines for designing low-leakage circuits in nanometre technology. Logic gate in the 70, 100, 130 and 180 nm technologies are simulated and analyzed. Stacking performs well as the threshold voltage decreases and hence aids further reduction of supply voltage and minimization of transistor sizes.

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